In the Claims

Claims are amended as follows:

1. (previously presented)   A comparator for an amplifier, the comparator comprising:

switch means which alternately (i) couples a first detector to the input of said amplifier and a second detector to the output of said amplifier and (ii) couples the first detector to the output of said amplifier and the second detector to the input of said amplifier, the amplifier output having been normalised to the amplifier input signal level and time aligned,

difference means arranged to determine an error value corresponding to the difference between said amplifier input and output;

digital signal processing means arranged to determine said error value as a function of said amplifier input signal level.

2. (previously presented)   A comparator as claimed in claim 1 wherein the difference means is a difference amplifier coupled to an output of said first detector and an output of said second detector.

3. (previously presented)   A comparator as claimed in claim 2 further comprising a DC offset applied to the output of one of said first detector and said second detector.

4. (previously presented)   A comparator as claimed in claim 1 wherein an output of said first detector and an output of said second detector are coupled to the digital signal processing means and the difference means is implemented by the digital signal processing means.

5. (currently amended)   A comparator as claimed in claim 1 wherein the switch means further comprises a 90 degree hybrid coupler and the comparator is operable

in a ~~wherein the switch means~~ phase detection mode in which the switch means couples the ~~comprises a switch matrix having a~~ 90 degree hybrid coupler ~~and arranged to switch the hybrid coupler~~ between said detectors and said amplifier input and said amplifier output such that said error represents phase error.

6. (currently amended)   A comparator as claimed in claim 1 wherein said difference means is arranged to determine a plurality of error values and said digital signal processing means averages said plurality of error values over a predetermined period for each said amplifier input signal level.

7. (previously presented)   A comparator and pre-distorter arrangement for an amplifier, the pre-distorter coupled to the input of the amplifier, and a gain/phase comparator coupled to the pre-distorter, the comparator having:

switch means which alternately (i) couples a first detector to the input of said amplifier and a second detector to the output of said amplifier and (ii) couples the first detector to the output of said amplifier and the second detector to the input of said amplifier, the amplifier output having been normalised to the amplifier input signal level and time aligned,

difference means arranged to determine an error value corresponding to the difference between said amplifier input and output;

digital signal processing means arranged to determine said error value as a function of said amplifier input signal level.

8. (currently amended)   An arrangement as claimed in claim 7 wherein the difference means is arranged to determine a plurality of error values and the pre-distorter averages the plurality of error values for each said amplifier input signal level.

9. (currently amended)   A comparator and pre-distorter arrangement for an amplifier, the pre-distorter coupled to the input of the amplifier, and a gain/phase comparator coupled to the pre-distorter, the comparator having:

switch means which alternately (i) couples a first detector to the input of said amplifier and a second detector to the output of said amplifier and (ii) couples the first detector to the output of said amplifier and the second detector to the input of said amplifier, the amplifier output having been normalised to the amplifier input signal level and time aligned,

difference means arranged to determine an error value corresponding to the difference between said amplifier input and output;

digital signal processing means arranged to determine said error value[[s]] as a function of said amplifier input signal level
and wherein the pre-distorter has gain or phase correction memory comprising gain or phase correction values as a function of amplifier input signal level, the pre-distorter being arranged to output said gain or phase correction values dependent on detected amplifier input; the pre-distorter further arranged to adapt said gain or phase correction values dependent on said error ~~values~~value determined by said comparator.

10. (original) An arrangement as claimed in claim 9 wherein the pre-distorter further comprises a second gain or phase memory comprising gain or phase correction values as a function of the amplifier input, the pre-distorter arranged to alternately switch between said first and second memory such that one said memory is used to output said correction signal whilst the correction values in the other memory are adapted.

11. (currently amended)   A method of determining the gain or phase error between the input and output of an amplifier, the method comprising:

detecting the input and output of said amplifier <u>by alternately (i) coupling a first detector to the input of said amplifier and a second detector to the output of said</u>

amplifier and (ii) coupling the first detector to the output of said amplifier and the second detector to the input of said amplifier, the amplifier output having been normalised to the amplifier input and time aligned, ~~wherein the means of detection are alternated between the amplifier input and output~~

determining an error value corresponding to the difference between the detected amplifier input and output;

. determining said error ~~values~~value as a function of amplifier input signal level.

12. (currently amended)   A method as claimed in claim 11 further comprising determining a plurality of error values and averaging said error values over a predetermined period.

13. (previously presented) An amplifier having a pre-distorter coupled to the input of the amplifier, and a gain/phase comparator coupled to the pre-distorter, the comparator having:

switch means which alternately (i) couples a first detector to the input of said amplifier and a second detector to the output of said amplifier and (ii) couples the first detector to the output of said amplifier and the second detector to the input of said amplifier, the amplifier output having been normalised to the amplifier input signal level and time aligned,

difference means arranged to determine an error value corresponding to the difference between said amplifier input and output;

digital signal processing means arranged to determine said error value as a function of said amplifier input signal level.

14. (previously presented) A base station comprising an amplifier having a pre-distorter coupled to the input of the amplifier, and a gain/phase comparator coupled to the pre-distorter; the comparator having:

switch means which alternately (i) couples a first detector to the input of said amplifier and a second detector to the output of said amplifier and (ii) couples the

first detector to the output of said amplifier and the second detector to the input of said amplifier, the amplifier output having been normalised to the amplifier input signal level and time aligned,

difference means arranged to determine an error value corresponding to the difference between said amplifier input and output;

digital signal processing means arranged to determine said error value as a function of said amplifier input signal level.

15. (new) A method as claimed in claim 11 further comprising applying a DC offset to the output of one of said first detector and said second detector.

16. (new) A method as claimed in claim 11 further comprising a preliminary step of applying the amplifier output and the amplifier input to a 90 degree hybrid coupler so that the determined error value is a phase error.

17. (new) A method as claimed in claim 11 further comprising determining a gain or phase correction value by using a look up table stored in a first memory, the method further comprising adapting a set of stored gain or phase correction values stored in a second memory dependent on said determined error value and alternately switching between the first memory and the second memory such that one of said memories is used to output said correction value whilst the correction values in the other memory are adapted.